What is claimed is:

1. A method comprising:

supplying a negative voltage to at least one deselected wordline of a memory array.

2. The method of claim 1, further comprising supplying a positive voltage to a selected wordline of the memory array to program the selected wordline while supplying the negative voltage.

3. The method of claim 2, further comprising supplying the negative voltage to all wordlines of the memory array except the selected wordline.

4. The method of claim 2, further comprising providing a second positive voltage signal to a selected bitline of the memory array.

5. The method of claim 4, further comprising reducing a leakage current through at least one deselected cell coupled to the selected bitline of the memory array.

6. The method of claim 1, further comprising providing the negative voltage and a control negative voltage to a decoder coupled to the at least one deselected wordline.

7. The method of claim 6, further comprising providing the control negative voltage to a substrate of a transistor of the decoder.

8. The method of claim 1, further comprising supplying the negative voltage at less than or equal to negative one volt.

9. The method of claim 1, further comprising supplying the negative voltage to the deselected wordline during a first time period, and supplying a positive voltage to the same wordline during a second time period to program memory cells coupled thereto.

10. An apparatus comprising:

a decoder to supply a negative voltage to a deselected address line of a memory array.

11. The apparatus of claim 10, wherein the decoder is further coupled to supply a positive voltage to the same address line if it is selected to be programmed.

12. The apparatus of claim 10, wherein the decoder comprises a first transistor having a well coupled to receive a negative control voltage, a source terminal

coupled to receive the negative voltage, and a drain terminal coupled to pass the negative voltage to the deselected address line.

13. The apparatus of claim 12, further comprising a second transistor coupled to the first transistor and the deselected address line to pass a program pulse to the deselected address line if it becomes a selected address line.

14. The apparatus of claim 12, further comprising a pre-driver circuit to disable the first transistor if the deselected address line becomes a selected address line.

15. The apparatus of claim 10, further comprising a plurality of memory cells coupled to the decoder via the deselected address line.

16. The apparatus of claim 15, wherein the plurality of memory cells comprise multi-level cells of a flash memory.

17. An article comprising a machine-readable storage medium containing instructions that if executed enable a system to:

supply a negative voltage to at least one deselected wordline of a memory array.

18. The article of claim 17, further comprising instructions that if executed enable the system to supply a positive voltage to a selected wordline of the memory array to program the selected wordline while the negative voltage is supplied to the at least one deselected wordline.

19. The article of claim 18, further comprising instructions that if executed enable the system to supply the negative voltage to all wordlines of the memory array except the selected wordline.

20. The article of claim 17, further comprising instructions that if executed enable the system to provide a negative control voltage to a substrate of a transistor coupled to pass the negative voltage to the at least one deselected wordline.

21. The article of claim 17, further comprising instructions that if executed enable the system to supply the negative voltage at less than or equal to negative one volt.

22. A system comprising:

a memory array having a plurality of memory cells each coupled to wordline and a bitline;

a decoder coupled to the memory array to supply a negative voltage to a deselected wordline of the memory array; and

a wireless interface coupled to the memory array.

23. The system of claim 22, wherein the decoder is further coupled to supply a positive voltage to the deselected wordline if it becomes a selected wordline.

24. The system of claim 22, further comprising a second decoder to supply a positive voltage to a selected wordline while the negative voltage is supplied to the deselected wordline.

25. The system of claim 22, wherein the decoder comprises a first transistor having a well coupled to receive a negative control voltage, a source terminal coupled to receive the negative voltage, and a drain terminal coupled to pass the negative voltage to the deselected wordline.

26. The system of claim 25, further comprising a second transistor coupled to the first transistor and the

deselected wordline to pass a program pulse to the deselected wordline if it becomes a selected wordline.

27. The system of claim 25, further comprising a pre-driver circuit to disable the first transistor if the deselected wordline becomes a selected wordline.

28. The system of claim 22, wherein the memory array comprises a flash memory.

29. The system of claim 28, wherein the flash memory comprises a multi-level cell flash memory.

30. The system of claim 22, wherein the wireless interface comprises an antenna.